

CLAIMS

1. An integrated circuit inductance structure, including:  
a silicon substrate;  
at least one planar winding of a conductive track;  
5 a resistive layer, not etched under the winding;  
a dielectric layer between the winding and said resistive layer; and  
discontinuous conductive sections, individually parallel to a closest portion of the  
winding, and electrically connected to ground and to said resistive layer.
- 10 2. The structure of claim 1, wherein said conductive sections are, for the most  
part, not arranged under projections of the winding.
3. The structure of claim 1, wherein each conductive section is placed as close  
as possible to the closest portion of the winding.
- 15 4. The structure of claim 1, wherein each portion of the winding is associated,  
along its length, to several conductive sections.
5. The structure of claim 1, wherein said conductive sections are connected to  
20 a contact point by several conductive tracks, each of the conductive tracks being arranged  
so that the resultant of the electromotive forces induced by the inductance is substantially  
null.
6. The structure of claim 5, wherein each of the conductive tracks  
25 substantially is an axis of symmetry of the inductance.
7. The structure of claim 1, wherein said conductive sections are formed in a  
same metallic level as a track forming an inductance.

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8. The inductance structure of claim 1, wherein said resistive layer has a doping level ranging between  $10^{16}$  and  $10^{19}$  atoms/cm<sup>3</sup>, preferably, on the order of  $10^{17}$  atoms/cm<sup>3</sup>.

Add  
a<sup>1</sup>

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